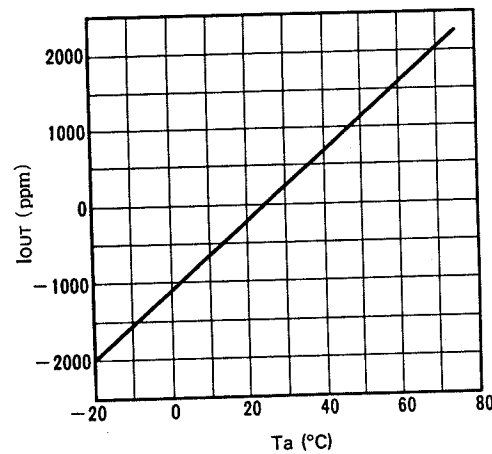
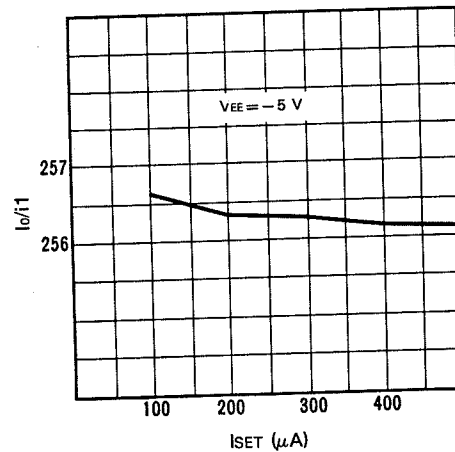


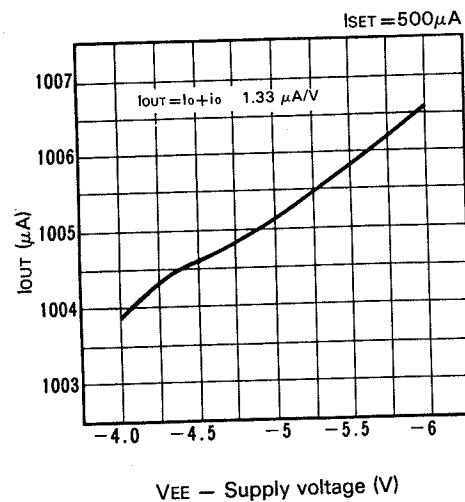
Temperature characteristics of I_{OUT} ($I_o + i_o$)
(R, Lch common)



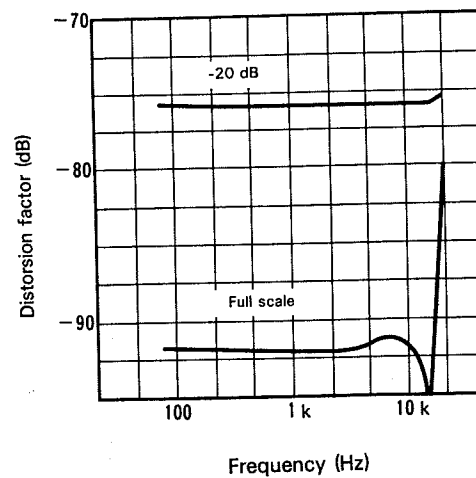
I_o/i_o vs. I_{SET}



Output current vs. Supply voltage (V_{EE})



Distortion factor



Dual 16 bit 88 kHz Multiplexed D/A

Description

CX20152 is a 16-bit D/A converter IC for PCM audio. It uses an integration system consisting of the following circuits.

- Clock signal generator
- TTL-ECL interface circuit
- Discharge drive circuit
- Analog switch drive circuit
- 1/4 frequency divider output circuit

By adding an integrator, analog switch and low pass filter externally to the IC, analog signal is reproduced from the 16-bit digital data.

Features

- Conversion frequency 88.2kHz
- Serial data input
- Low distortion factor 0.003% (typ.)
- 1/4-division output of the master clock is available for the clock of the CX23035, a single-chip LSI for CD, and the digital filter CX23034.

Structure

Bopolar Silicon Monolithic IC

Absolute Maximum Rating

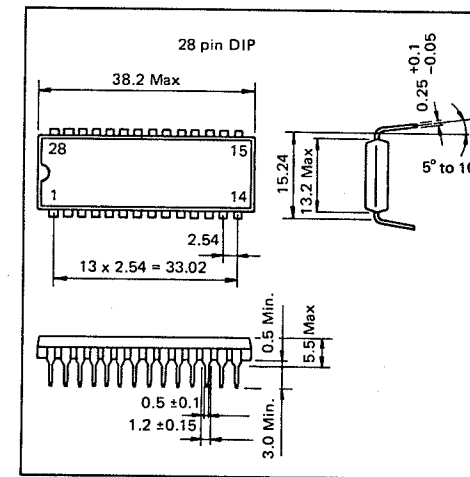
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	-20 to +75	°C
• Storage temperature	T_{stg}	-55 to +150	°C
• Allowable power dissipation	P_d	2.1	W

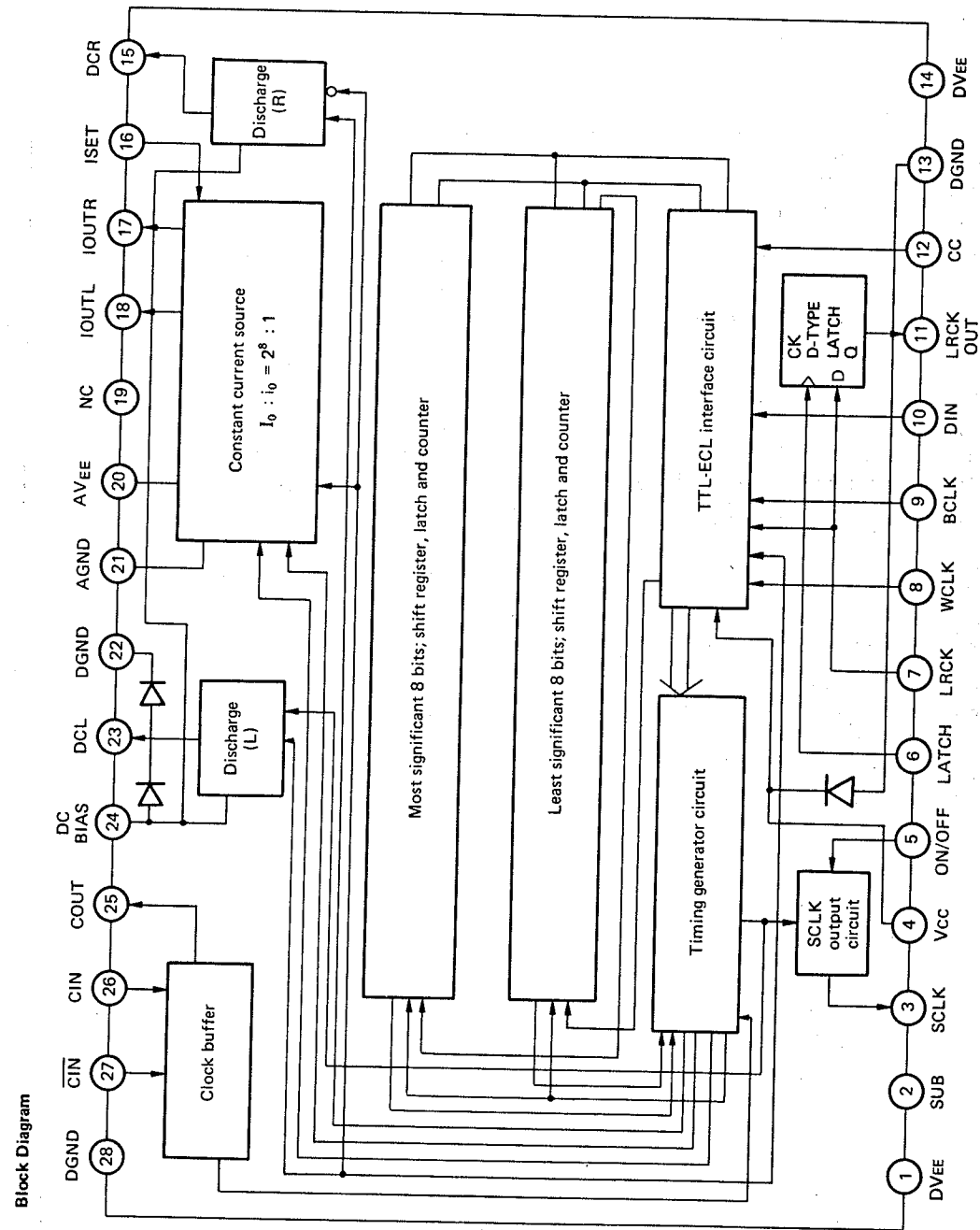
Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V
	V_{EE}	-5 ± 0.25	V

Package Outline

Unit: mm





Block Diagram

Pin Description

No.	Symbol	Description
1	DVEE	Digital VEE: -5V
2	SUB	IC substrate: Be sure to connect to Pin 1.
3	SCLK	System clock output pin
4	Vcc	Digital Vcc: +5V
5	ON/OFF	Pin to determine the system clock on/off
6	LATCH	Clock pin of D type latch
7	LRCK	LRCK input pin
8	WCLK	WCLK input pin
9	BCLK	BCLK input pin
10	DIN	DIN (data input pin): MSB first
11	LRCK OUT	LRCK output pin
12	CC	CC input pin
13	DGND	Digital ground
14	DVEE	Digital VEE: -5V
15	DCR	Right channel discharge drive signal output pin
16	ISET	Integration current setting pin
17	IOUTR	Right channel current output pin
18	IOU TL	Left channel current output pin
19	NC	No connection
20	AVEE	Analog VEE
21	AGND	Analog GND
22	DGND	Digital GND
23	DCL	Left channel discharge drive signal output pin
24	DC BIAS	Discharge circuit bias pin
25	COUT	Clock generator output pin
26	CIN	Clock generator positive input pin
27	CIN	Clock generator negative input pin
28	DGND	Digital GND

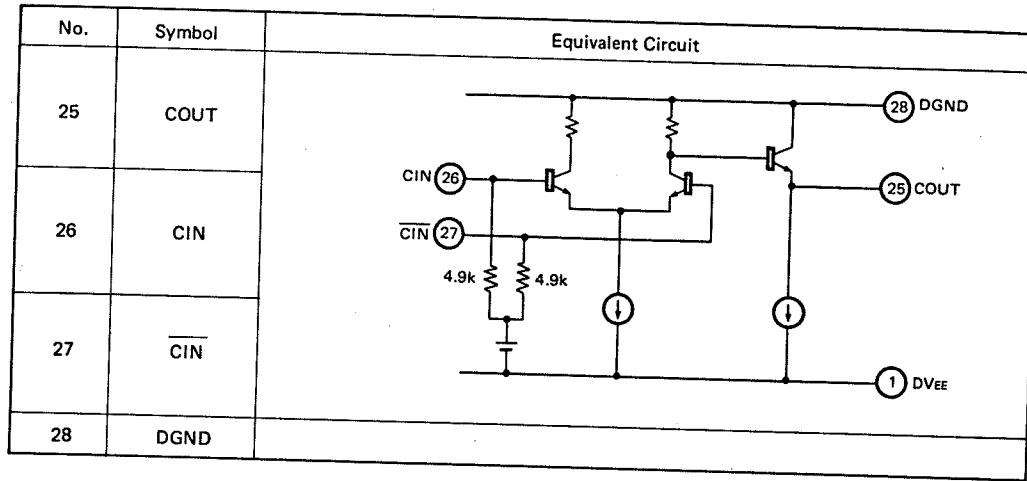
CX20152 Input/Output Pin Equivalent Circuits

No.	Symbol	Equivalent Circuits
1	DVEE	
2	SUB	
3	SCLK	
4	VCC	
5	ON/OFF	

No.	Symbol	Equivalent Circuit
6	LATCH	
7	LRCK	
8	WCLK	
9	BCLK	
10	DIN	
12	CC	

No.	Symbol	Equivalent Circuits
11	LCK OUT	
13	DGND	
14	DVEE	
15	DCR	
23	DCL	
24	DC BIAS	

No.	Symbol	Equivalent Circuits
22	DGND	
16	ISET	
17	IOUTR	
18	IOUTL	
19	NC	
20	AVCE	
21	AGND	



Electrical Characteristics

(Ta = 25°C, VEE = -5.0V, VCC = 5.0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Circuit current	IEE	1, 2, 14, 20 Pins 4, 5 = 5V	-125	-95		mA
Circuit current	ICC1	4 Pin 5 = 5V (6, 7, 8, 9, 10, 12, GND)		12.6	15.5	mA
Circuit current	ICC2	4 Pin 5 = 0V (6, 7, 8, 9, 10, 12, GND)		5.9	10.0	mA
Input threshold voltage	VTH	6, 7, 8, 9, 10, 12		2.1		V
High level input voltage	VIH	6, 7, 8, 9, 10, 12			0.9	V
Low level input voltage	VIL	6, 7, 8, 9, 10, 12				V
High level input current 1	IHI1	5 VIH = 5V		0.7	1.3	mA
High level input current 2	IHI2	6, 7, 8, 9, 10, 12 VIH = 5V		250	550	μA
Low level input current 1	ILI1	5 VIH = 0V		0.35	0.8	mA
Low level input current 2	ILI2	6, 7, 8, 9, 10, 12 VIL = 0V		120	550	μA
High level output voltage	VLACKH	11 With Pin 7 at 4.5V, set IOH = -100μA and input a clock of 0V-5V-0V to Pin 6.	2.7	4.2		V
Low level output voltage	VLACKL	11 With Pin 7 at 0V, set IOL = 100μA and input a clock of 0V-5V-0V to Pin 6.		-3.1	-2.7	V
SCLK output, high level	VSCLKH	3 IOH = -10μA	3.4	4.2		V
SCLK output, low level	VSCLKL	3 IOL = 400μA		0.5	1.6	V
Discharge circuit power dissipation current	IDCBIAS	24 VDCBIAS = 0V		1.9	2.5	mA
Discharge circuit high level output voltage	VDCH	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA	0	0.4	0.65	V
Discharge circuit low level output voltage	VDCL	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA		-4.2	-3.4	V
ISET current	ISET	16		0.5	1.0	mA
IOUT output current	IOUT	17, 18 Pins 17, 18: Voltage = 0V Pin 16: ISET = 500μA (IOUT = IO + IO)		2.008		mA
Clock input bias voltage	VCIN	26, 27		-1.3		V
Clock high level output voltage	VCOH	25		-0.8		V
Clock low level output voltage	VCOL	25		-1.6		V
Current output pin leakage	IO LEAK	17, 18 Pins 17, 18: Voltage = 0V when the current output is off.			1.5	μA
Current ratio	IO/IO	17, 18 Pin 16: ISET = 500μA	255.0	256.0	257.5	-
Distortion factor	THD1	Both right and left: 0dB (full scale) when reproduced.		0.003	0.005	%
	THD2	Both right and left: -20dB when reproduced.		0.02	0.025	%
Operation clock frequency	fCLK1	Both self-drive & external-drive Ta = -20 ~ +70°C		68	80	MHz
Operation clock frequency	fCLK2	Both self-drive & external-drive Ta = -20 ~ +75°C		68	75	MHz

Description of Conversion Operation

(1) Data pickup (BCLK, DIN, WCLK, LRCK)

Data consist of 16-bit serial signals in 2's complement. They are transmitted into the IC sequentially from the MSB in synchronization with the rise edge of the bit clock (BCLK). (The BCLK delay will change the data. The falling edge changes the data.)

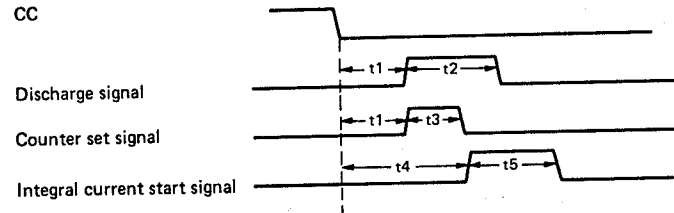
When the word clock (WCLK) is changed from high level to low level at the 17th BCLK, the 16-bit data is transferred from the shift register to the latch with the decay signal. When CX20152 is used in the stereo mode, other-channel data are transmitted from the 17th BCLK.

In the stereo mode, the Rch data is picked up when LRCK is at a low level and the Lch data is picked up when LRCK is at a high level. IOU TL and DCL operate only when LRCK is at a low level, and IOU TR and DCR operate only when LRCK is at a high level.

(2) Conversion operation (CC, LRCK, CIN, IOU TL, IOU TR, DCL, DCR)

When more than 3 clocks are fed from the clock input (CIN) with the conversion command (CC) at a high level, all the internal timing circuits are reset.

After the resetting, the internal timing circuit starts operation when a clock is input from CIN with CC at a low level. From this operation, three signals, Discharge, Counter set and Integral current Start, are generated. Timing of these signals is determined as follows by the clock interval τ_0 and its quantity.



$$t1 = 35 \times \tau_0$$

$$t2 = 67 \times \tau_0$$

$$t3 = 31 \times \tau_0$$

$$t4 = 65 \times \tau_0$$

$$t5 \text{ Min} = 47 \times \tau_0 \quad (\text{When the input data is } 01 - 1)$$

$$t5 \text{ Max} = 302 \times \tau_0 \quad (\text{When the input data is } 10 - 0)$$

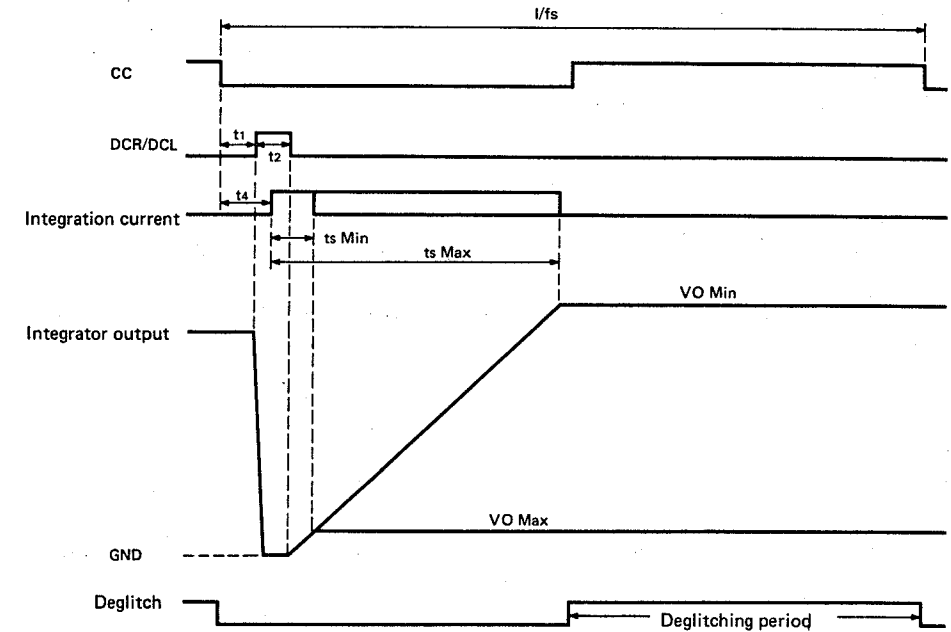
The counter set signal is used to set the data input in the latch to the counter but does not output externally.

The discharge signal is output from DCL and DCR and controlled by LRCK. It is output from DCL when LRCK is at a low level and from DCR when LRCK is at a high level.

The integral current start signal starts the upper current i_0 and lower current i_1 flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, counts 11 offsets after the end of the counting and outputs a signal to stop the integration current. The value t_5 is varied between 0 to 255 by the input data value preset to the counter.

Therefore, the time before the end of the integration after the low level has been set, i.e. the conversion time, requires the maximum ($t_4 + t_5 \text{ Max} = 367 \times \tau_0$) seconds.

The integration current of IOU TL is output, as with the discharge signal, when LRCK is at a low level; IOU TR is output when LRCK is at a high level.

(3) The relation between sampling frequency f_s and clock

The maximum and minimum values of the integration voltage output, $V_{O \text{ Max}}$ and $V_{O \text{ Min}}$, are expressed as follows.

$$V_{O \text{ Max}} = \frac{i_0}{C} \cdot \tau \cdot 267 + \frac{i_1}{C} \cdot \tau \cdot 266 \quad (t_4 + t_5 \text{ Max})$$

$$V_{O \text{ Min}} = \frac{i_0}{C} \cdot \tau \cdot 12 + \frac{i_1}{C} \cdot \tau \cdot 11 \quad (t_4 + t_5 \text{ Min})$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency f_s and the clock frequency f_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$f_s = \frac{f_{\text{CLK}}}{2 \times (t_4 + t_5 \text{ Max})} = \frac{f_{\text{CLK}}}{734}$$

where $f_s = 44.1 \text{ kHz}$ results in 32.4 MHz of f_{CLK}

It is, however, recommendable to specify f_s as the follow for the practical use because a settling time of 0.5 to 1.0 μ s is required for the integrator after the current for t_s disappears:

$$f_s = \frac{f_{CLK}}{(t_4 + t_s \text{ Max} + 1.0(\mu\text{s}) + T)}$$

(4) Integration current setting (ISET, IOUTL, IOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$I_{OUTL(R)} = I_0 + i_0 = (4 + \frac{1}{64}) I_{SET}$$

where i_0 and I_0 are integration currents corresponded to the 1LSB and 2^8 -LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_0 is given by the following equation:

$$V_0 = \frac{I_0}{C} (D_0 * 2^7 + \bar{D}_1 * 2^7 + \dots + \bar{D}_7 * 2^0 + 12) \tau_0 \\ + \frac{i_0}{C} (\bar{D}_8 * 2^7 + \bar{D}_9 * 2^6 + \dots + \bar{D}_{15} * 2^0 + 11) \tau_0$$

where $I_{SET} = 500 \mu\text{A}$, $\tau = \frac{1}{35 \text{ (MHz)}} = 28.6 \text{ (ns)}$ and $C = 2000 \text{ pF}$ result in the maximum output voltage $V_{O \text{ Max}}$

of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$$I_0 = 4 * I_{SET}$$

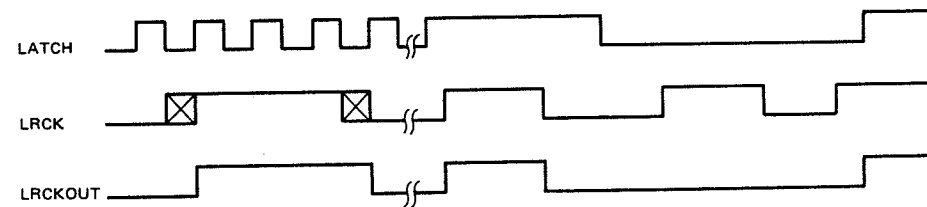
$$i_0 = \frac{1}{64} * I_{SET}$$

$V_{O \text{ Max}}$ is calculated as the follow:

$$V_{O \text{ Max}} = \frac{2.0 * 10^{-3}}{2000 * 10^{-12}} * 267 * 28.6 * 10^{-9} \\ + \frac{400 * 10^{-6} / 64}{2000 * 10^{-12}} * 266 * 28.6 * 10^{-9} \\ = 7.67 \text{ (V)}$$

(5) LRCK OUT operation (LATCH, LRCK, LRCK OUT)

The LRCK OUT is a drive output of the analog switch IC (equivalent to MC14053B) to clip the output converted by CX20152 and the integrator so that the converted output can be a PAM wave. When the PAM wave has a jitter, a conversion error results. To absorb this jitter, a D-type latch is built-in and the LATCH input is used as its clock. The D-type latch varies the output state in synchronization with the rise of the clock. In the high-speed conversion (with sampling frequency of 88.2kHz), the clock frequency is as high as about 70MHz. This will affect the delay time of the analog switch IC; it is possible the delay time becomes equal to t_1 . Then, the last part of the PAM wave overlaps on the discharge time causing a considerable conversion error. In such a case, LRCK can output its level by keeping LATCH at a high level. The output voltage level ranges from -2.7V to +2.7V, enable to drive CMOS analog switch.



Timing of LATCH, LRCK and LRCKOUT

(6) Clock input/output Pin (COUT, CIN and \bar{CIN})

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased with an internal bias circuit (= -1.3V). The output amplitude level is 0.8V.

(7) Bias Pin (DV_{EE}, SUB, DGND, V_{CC}, AV_{EE}, AGND and DC BIAS)

SUB denotes the IC substrate and its voltage potential should be common to that of DV_{EE}. The standard value of DV_{EE} and AV_{EE} is -5.0V.

V_{CC} is the power supply for the interface circuit from a CMOS or TTL level to the internal ECL logic. Its standard value is +5V.

DC BIAS is the bias circuit of the discharge signal output circuit. As it requires about 2.5mA as its standard current, supply current should be 2.5mA + α . This pin voltage is biased to 2Vf and the value of α is determined as follows.

To maintain the pin voltage at 2Vf (≈ 1.4 V), about 0.5 mA of current is required. Additionally, the maximum current flowing through the load resistor R_L attached to DCR (Pin 15) and DCL (Pin 23) is obtained from the following equation.

$$1/R_L \times (V_{DCH} + |DV_{EE}|) \times 2, \text{ where } R_L = 4.7\text{kohm}, V_{DCH} = 0.4\text{V and } DV_{EE} = -5\text{V}$$

Hence, $\alpha = 0.5 + 1.32 = 1.82 \text{ (mA)}$

Therefore, the total current will be 4.32mA.

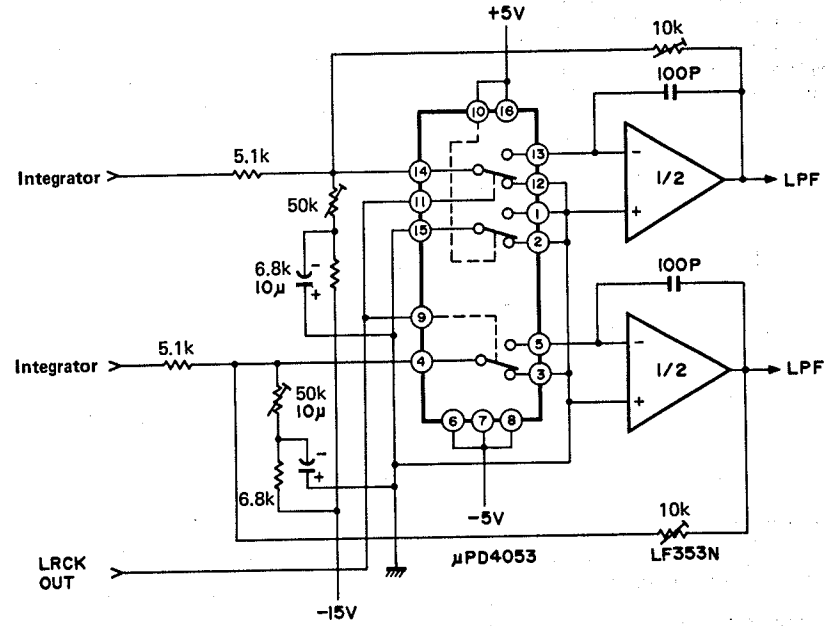
We recommend 5mA with R_L at 4.7 k Ω .

(8) System clock output pin, ON/OFF (SCKL, ON/OFF)

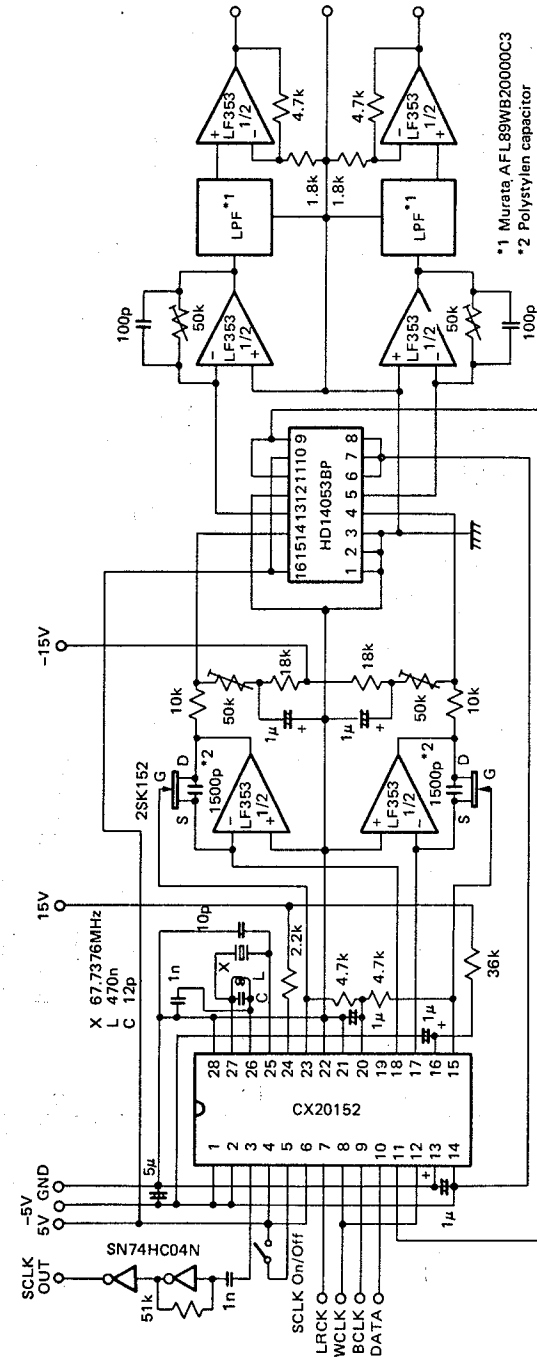
SCLK is the output pin of the 1/4 frequency divider of the oscillation circuit's master clock frequency. The frequency outputs when the ON/OFF pin is supplied with 5V (V_{CC}) and stops when the ON/OFF pin is supplied with 0V or set to open.

As its output amplitude is 2V and too low to be connected directly to a TTL or CMOS, be sure to amplify before connection.

Application Circuit for Operating Deglitcher in Sample/Hold Type

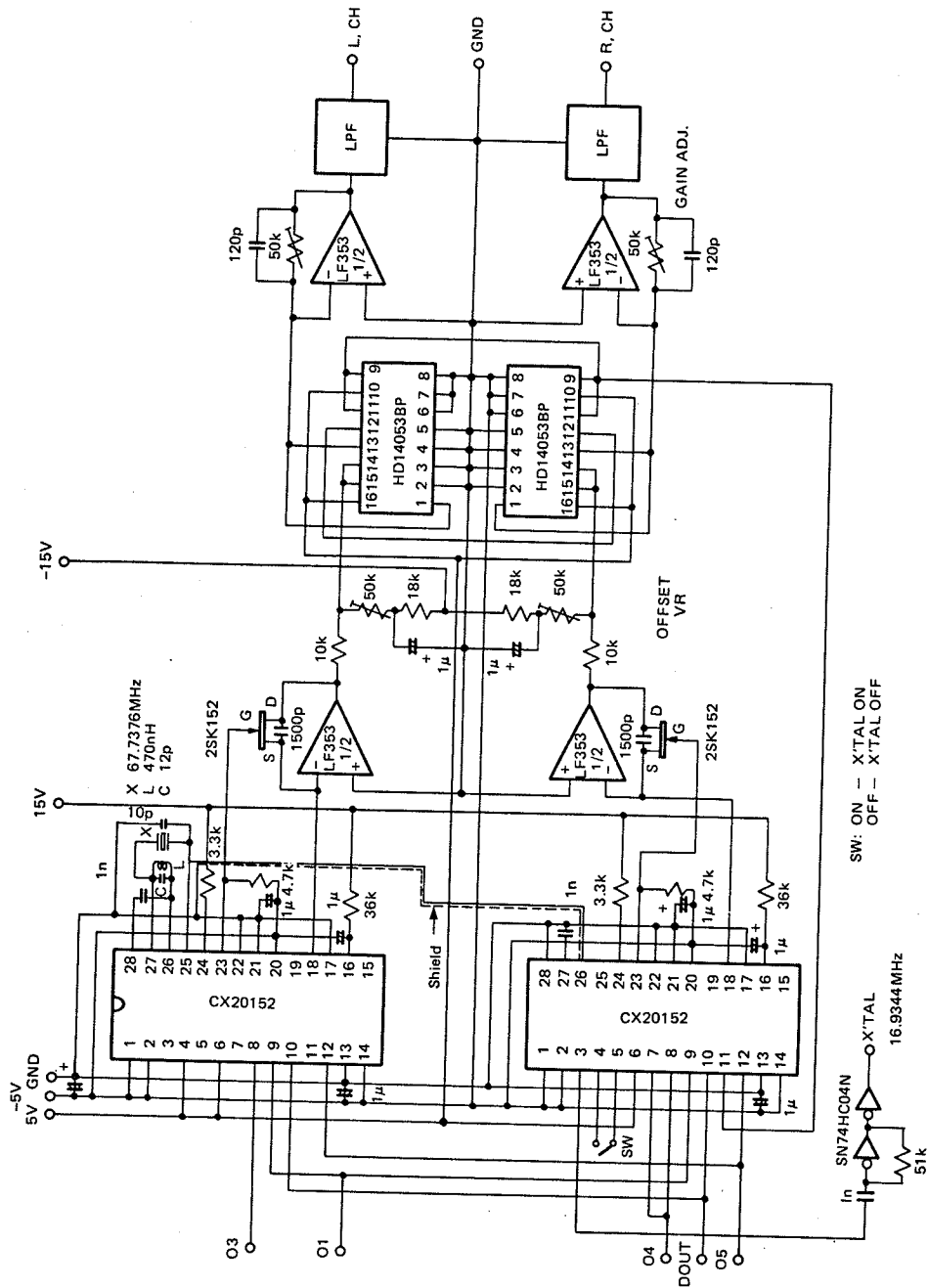


Application Circuit (Example 1)

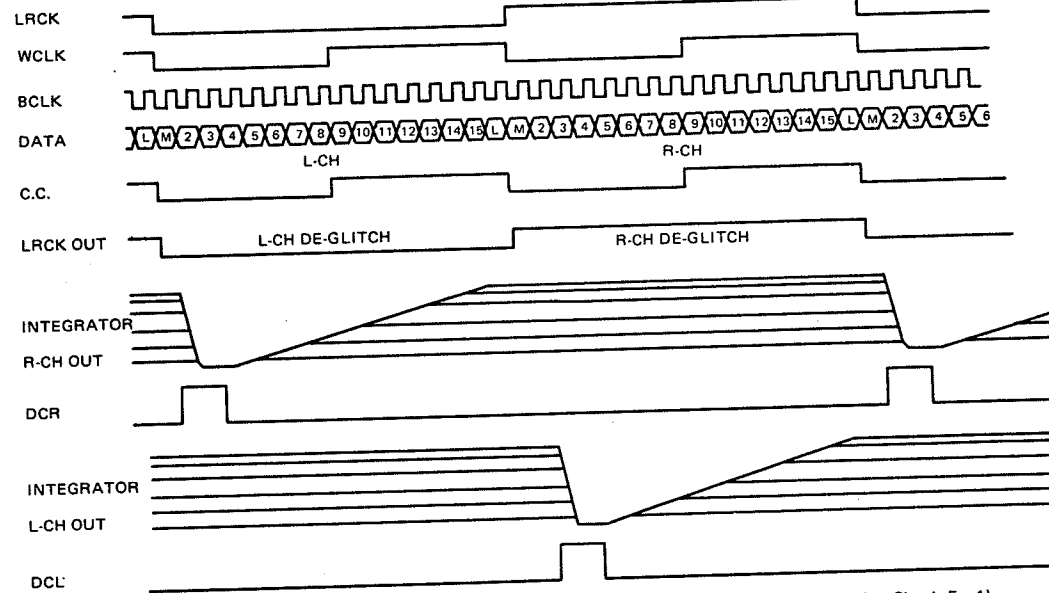


*1 Murata AFL89WB20000C3
*2 Polystylen capacitor

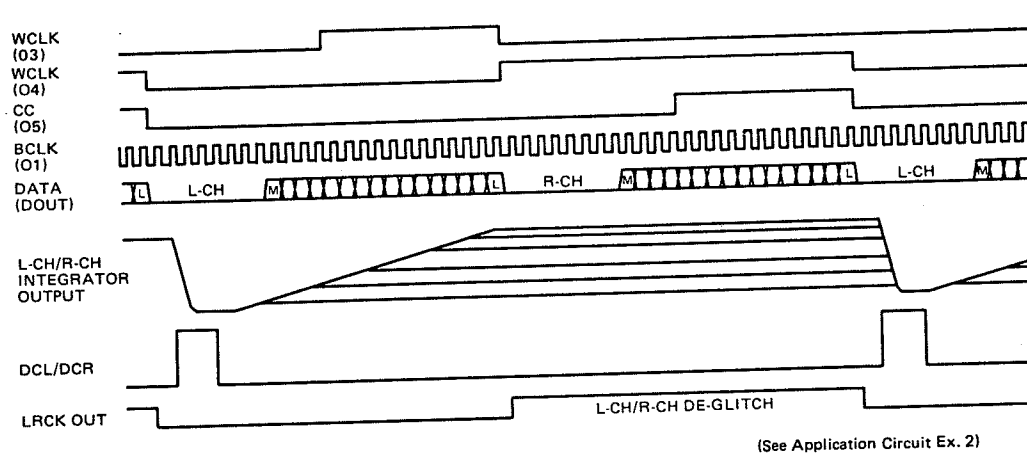
Application Circuit (Example 2)



Timing Chart

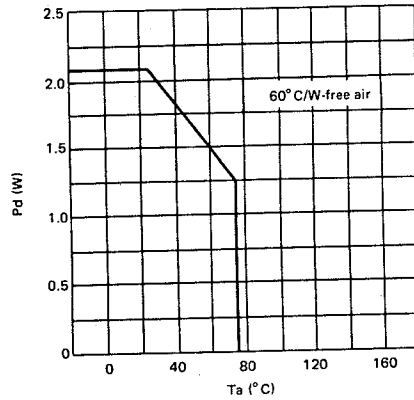


Timing Chart II

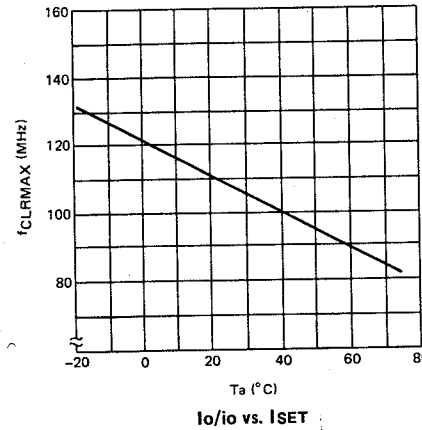


Dual 10 bit 50 KHz Multiplexed A/D + D/A

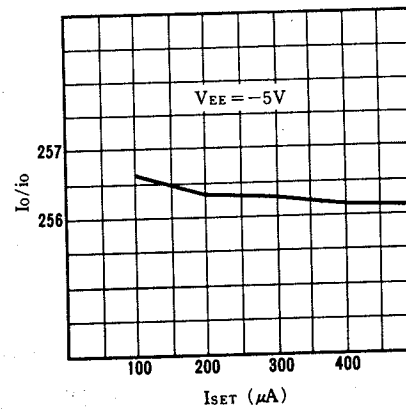
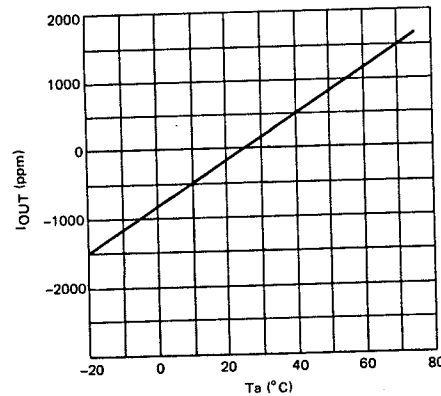
Maximum allowable power dissipation decrement curve



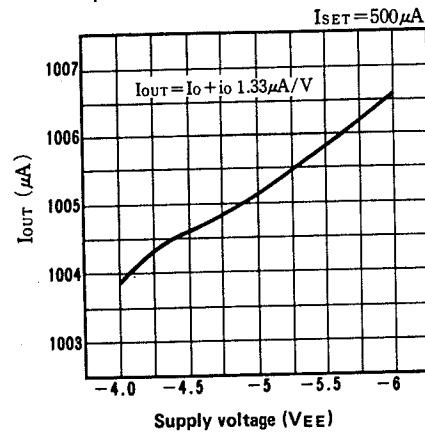
Maximum clock frequency temperature characteristics



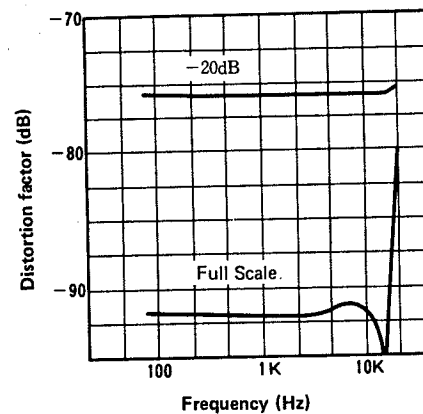
Input temperature characteristics (Io + io) (Both of R, Lch)



Output current vs. Supply voltage (VEE)



Distortion factor



Description

The CX23010/CX23060 are the 10 bit, 50 kHz CMOS A/D, D/A Converters for Audio digital signal processing, using a coarse-fine integration technique. Both Analog to Digital and Digital to Analog Conversions are capable with selecting the mode. It can be separated into 2 blocks. One is a digital block includes

- Digital block includes
 - A digital limiter
 - A counter
 - A timing generation circuit
- Analog block includes
 - A current source
 - An operational amplifier
 - A comparator
 - A multiplexer (2-channel)

Features

- A Single Power Supply: $V_{DD} 5V$
- Minimum number of external parts required (Around one-third compared with our current A/Ds)
- Two channel audio A/D, D/A processing (L and R Channels)
- 2's Complementary digital code is employed
- Low Power consumption (Less than 50 mW)

Structure

- Silicon Gate CMOS IC

Applications

- Digital Audio Signal Processing
- PCM Audio Processing
- Telecommunications Digitizing
- Computer Interface System

Absolute Maximum Ratings ($T_a = 25^\circ C$)

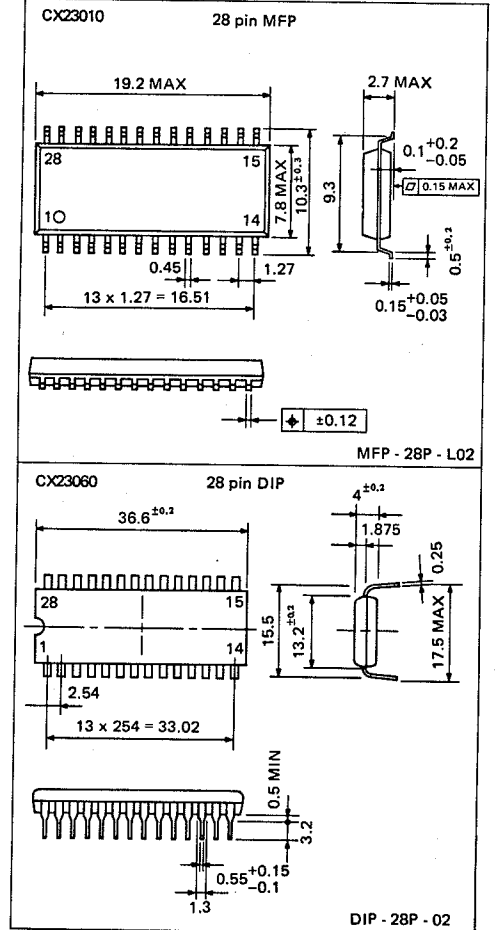
- Supply voltage V_{DD} -0.3 to 7.0 V
- Analog input voltage V_{IN} -0.3 to $V_{DD} + 0.3$ V
- Operating temperature T_{opr} -20 to +75 °C
- Storage temperature T_{stg} -55 to +150 °C
- Allowable power dissipation
 - P_D 650 mW for CX23010
 - P_D 800 mW for CX23060

Recommended Operating Conditions

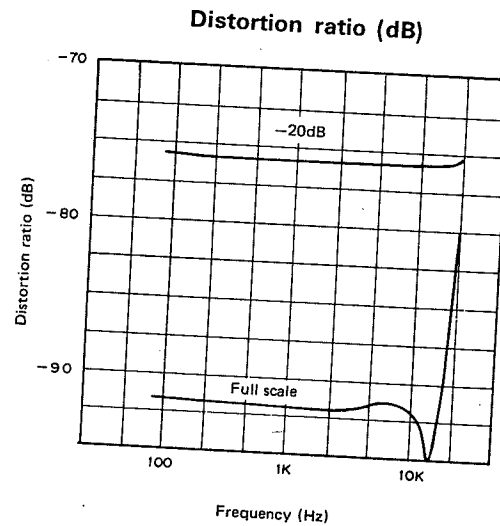
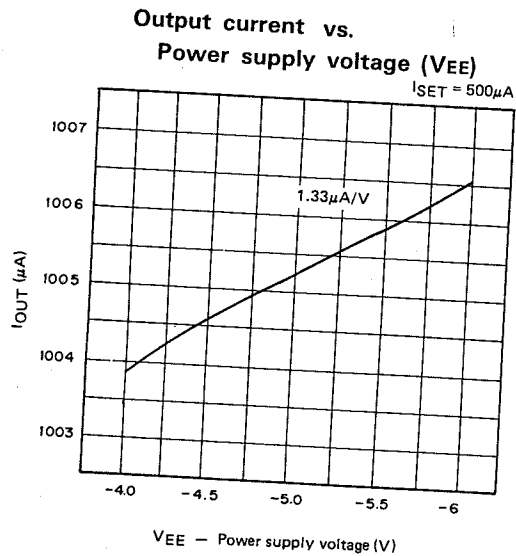
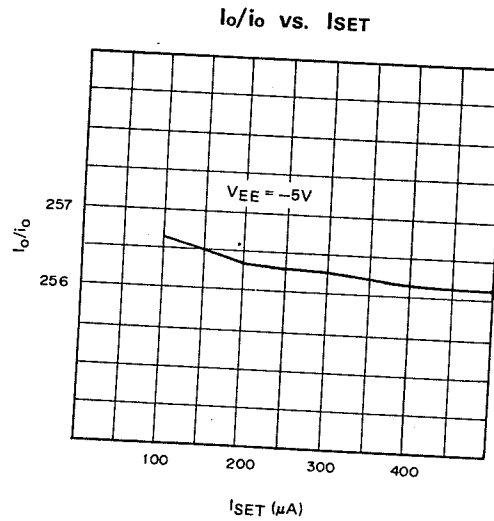
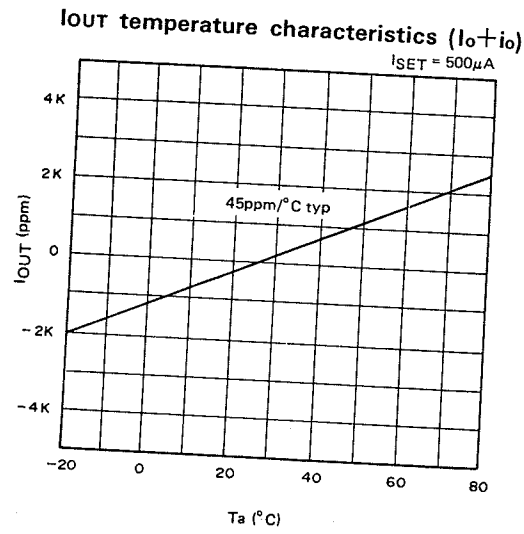
- (1) AV_{DD}, DV_{DD} 4.5 to 5.5 V
- (2) $AV_{DD} \leq DV_{DD}$ 0.5 V

Package Outline

Unit: mm



Dual 16 bit 44 kHz Multiplexed A/D Converter



Description

The CX20018 is a monolithic bipolar IC designed for PCM (Pulse Code Modulation) audio. This IC consists of 16 bit counters, shift registers, clock buffer, clocked synchronous comparator, stabilized current source and TTL compatible interface circuits, etc.

Features

- Line monotonicity
- Low noise
- TTL compatible input/output
- Stereo or monaural modes can be selected by external control

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

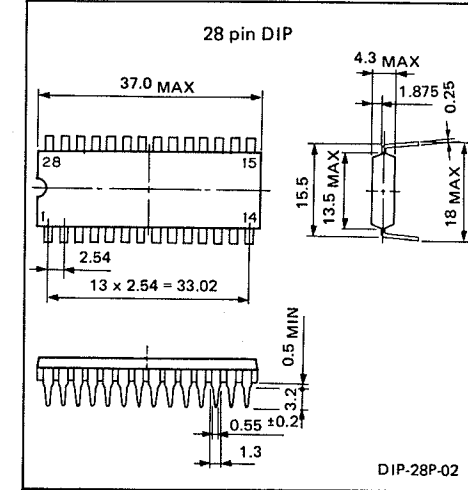
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	-20 to +75	°C
• Storage temperature	T_{stg}	-50 to +150	°C
• Allowable power dissipation	P_D	1.7	W

Recommended Operating Conditions

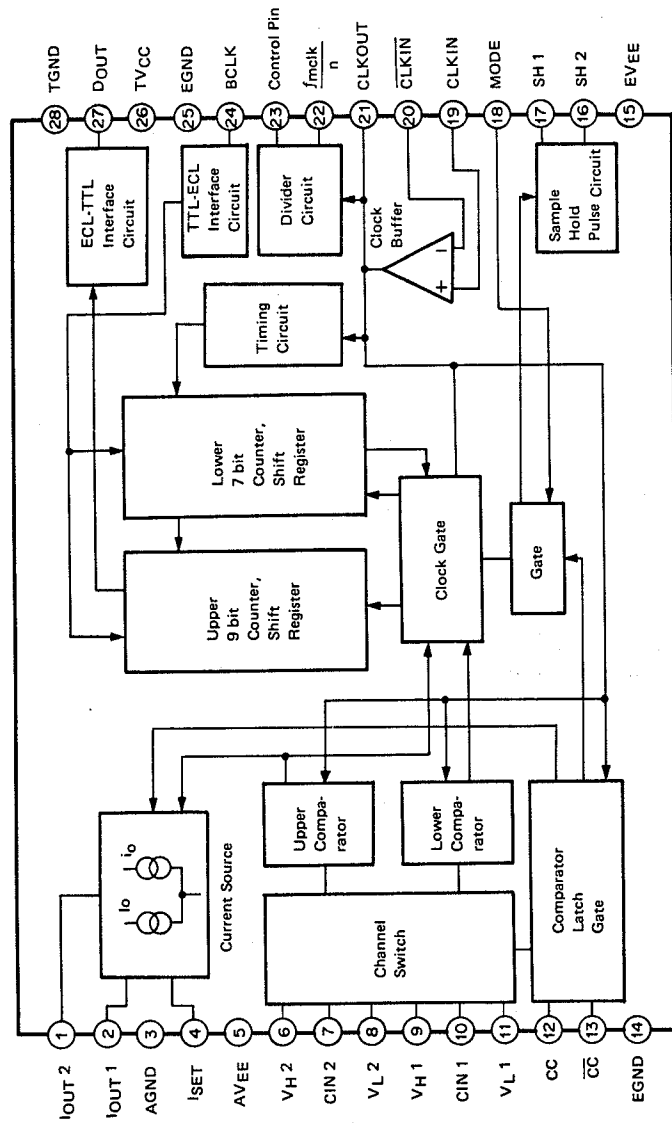
• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	-5.25 to -4.75	V

Package Outline

Unit: mm



Block Diagram



Electrical Characteristics

(Ta=25°C, VEE=-5V, VCC=5V)

Item	Symbol	Pin No. and Test Conditions	Min.	Typ.	Max.	Unit	Note
Supply Voltage Range *1	VEE		-4.75	-5.00	-5.25	V	1
Supply Voltage Range *1	VCC		4.75	5.00	5.25	V	1
Circuit Current	IEE		70.0	102.0	130.0	mA	1
Circuit Current	ICC		4.0	10.0	15.0	mA	1
Current Output Pin Leak	I _{OLEAK}	1, 2 (Pins 1, 2 Voltage=0V when current output is off)			1.0	μA	2
I _{out} Output Current	I _{out}	1, 2 (Pins 1, 2 Voltage=0V, I _{set} =410 μA)		1.64		mA	2
Current Ratio *2	I _o /I _{io}	1, 2 (I _{set} =410 μA)	127.0	128.0	129.0		2
Maximum I _{SET} Current	I _{SET} Max.	4 127.0 ≤ I _o /I _{io} ≤ 129.0			750	μA	2
Sample Hold Pulse High Level Output Voltage	V _{SH1H} V _{SH2H}	16, 17	-0.05	0	0.1	V	
Sample Hold Pulse Low Level Output Voltage	V _{SH1L} V _{SH2L}	16, 17	-4.40	-4.25	-3.50	V	
Clock Input Bias Voltage	V _{CLKIN} V _{CLKIN}	19, 20	-1.90	-1.72	-1.50	V	
Clock Output Low Level Output Current	I _{CLKOUTL}	21		3.0	4.0	mA	
CC, CC Input Bias Voltage	V _{CCIN} V _{CCIN}	12, 13	-2.20	-1.92	-1.60	V	
Data Output High Level Output Voltage	V _{DOUTH}	27 I _{OH} =0.1 mA	3.2			V	
Data Output Low Level Output Voltage	V _{DOUTL}	27 I _{OL} =-0.4 mA			0.4	V	
Bit Clock High Level Input Voltage	V _{BCLKH}	24	2.0			V	
Bit Clock Low Level Input Voltage	V _{BCLKL}	24			0.5	V	
Bit Clock High Level Input Current	I _{BCLKH}	24		4		μA	
Bit Clock Low Level Input Current	I _{BCLKL}	24	0.2	1		μA	
Distortion *3 Factor	THD	During 0 dB (full scale) playback for both channel		0.005	0.006	%	3
		During -20 dB playback for both channel			0.05	%	3

Item	Symbol	Pin No. and Test Conditions	Min.	Typ.	Max.	Unit
Maximum Operating Clock Frequency	fMCLK	Self-excitation or separate excitation			100	MHz
Dividing Ratio Control Voltage	VCTL (∞)	23	2.0	5.0	V	
	VCTL (2)	23	0.2	0.8	V	
	VCTL (4)	23	-0.8	-0.2	V	
	VCTL (8)	23	-5.0	-2.0	V	
Mode Control Voltage	VMODE (1)	18 Stereo, S/H ON	2.0	5.0	V	
	VMODE (2)	18 Stereo, S/H OFF	0.2	0.8	V	
	VMODE (3)	18 Monaural, S/H OFF	-0.8	-0.2	V	
	VMODE (4)	18 Monaural, S/H ON	-5.0	-2.0	V	

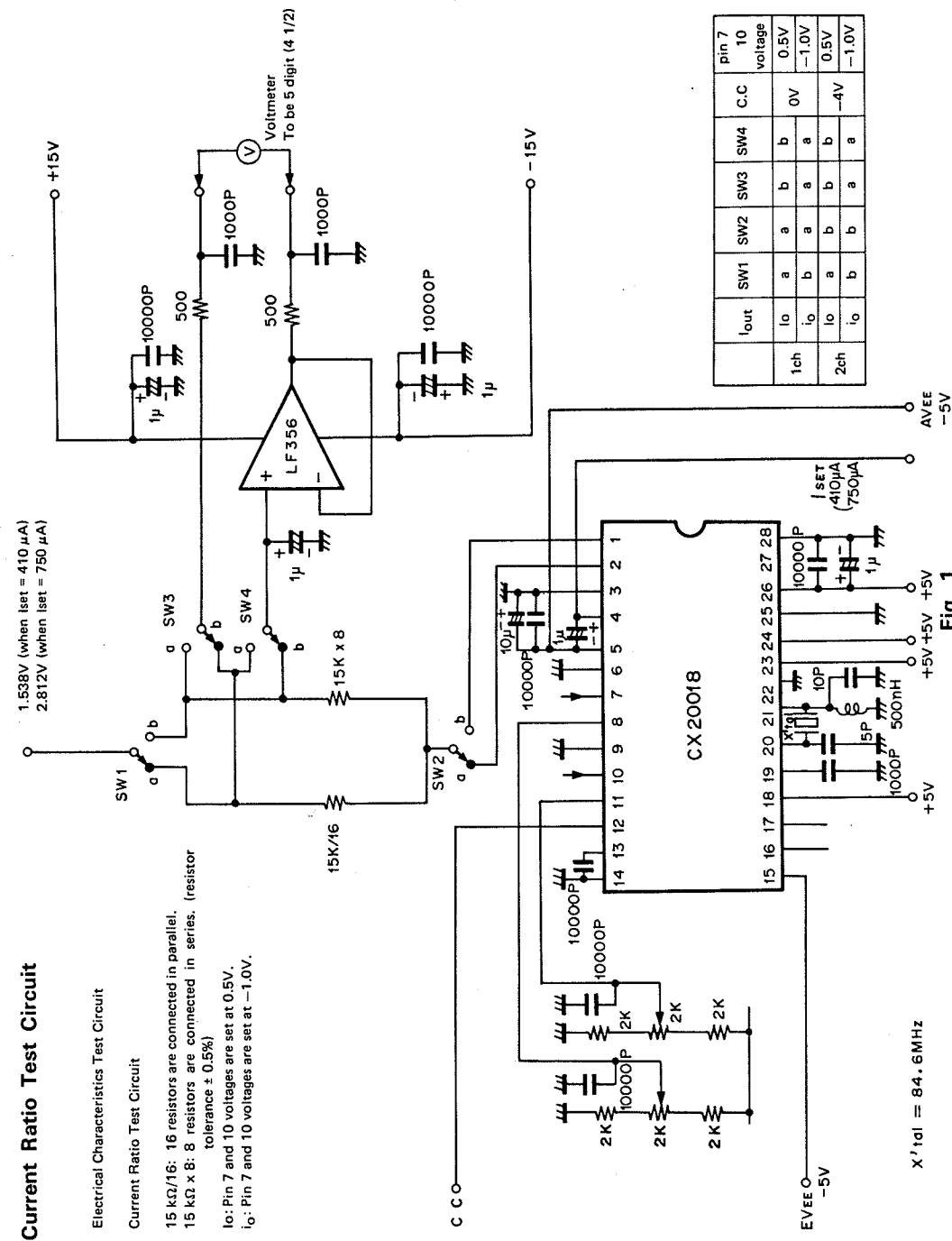
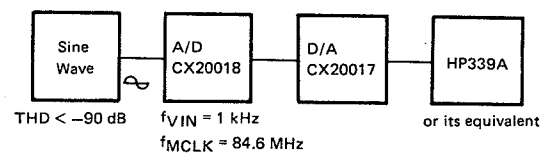
- Note** 1 Pins 1, 2, 3, 6, 7, 8, 9, 10, 11, 14, 21, 25 and 28 are for grounding, pins 18, 22, 23, are connected Vcc. Pin 4 draws 410 μA of current by external current source.
 2 Reference to the current ratio test circuit.
 3 Conversion Frequency 44.1 kHz
 Distortion Meter HP339A (all Filters are turned on) or its equivalent that has an 80 kHz, LPF, 30 kHz LPF and 400 Hz HPF.

*1 Recommended operating voltage

*2 In the current ratio test circuit (See Fig. 1)

$$\left| 15 \times 8 \text{ (k}\Omega\text{)} \times i_o \text{ (}\mu\text{A)} - \frac{15}{16} \text{ (k}\Omega\text{)} \times i_o \text{ (}\mu\text{A)} \right| < 12.0 \text{ mV}$$

*3 Measurement Method (See Note 2)



Current Ratio Test Circuit

Electrical Characteristics Test Circuit

Current Ratio Test Circuit

15 kΩ/16: 16 resistors are connected in parallel.
 15 kΩ x 8: 8 resistors are connected in series. (resistor tolerance ± 0.5%)

Io: Pin 7 and 10 voltages are set at 0.5V.

Io: Pin 7 and 10 voltages are set at -1.0V.

X'1d1 = 84.6MHz

Fig. 1

Description of CX20018 Conversion Process

Conversion process

The timing circuit controls a conversion cycle and send "Data Transfer Pulse" to the 16 bit shift register for transmitting the last converted data. It is reset by both the edge of CC (Conversion Command), and the master clock pulse is fed to the timing circuit.

"Data Transfer Pulse" and "Mask Pulse" become "H" level as soon as the timing circuit starts to count clocks. "Data Transfer Pulse" becomes "L" when the timing circuit counts 11 clocks, and then the last data is transferred. Simultaneously, "Current Switch Pulse" becomes "H", and integral current starts to flow. "Counter Preset Pulse" becomes "H" when the timing circuit counts 16 clocks. And then, upper and lower level counters are reset. Counter Preset Pulse holds "H" level during the period of 8 clocks.

When the timing circuit counts 31 clocks, Mask Pulse becomes "L" and A/D conversion starts. The coarse current "I_{co}" discharges the sampled charge of integrator until the output voltage of integrator crosses the reference voltage (V_{refH}). During this period the upper level counter counts the number of clock. After crossing the V_{refH} the fine current discharges the remaining charge of integrator. The lower level counter counts the number of clock until the output voltage of integrator crosses the lower level references voltage (V_{refL}). (See Figs. 2, 3, 4)

Data output

Data are 16 bit serial signals and 2's complement. The serial data are synchronous with a rising edge of Bit clock (BCLK), and only MSB data is synchronized with a edge of "Data Transfer Pulse". (See Fig. 3)

Monaural operation mode

In monaural mode the external integrator is tracking the input signal during CC is "H" state. At the moment when CC goes "L" state, the CX20018 starts conversion. The data is transferred to the output from MSB sequentially.

After 16 bit data are transferred, "Data Out" comes to the "H" level and keeps "H" level until next conversion. (See Fig. 4)

Timing Chart

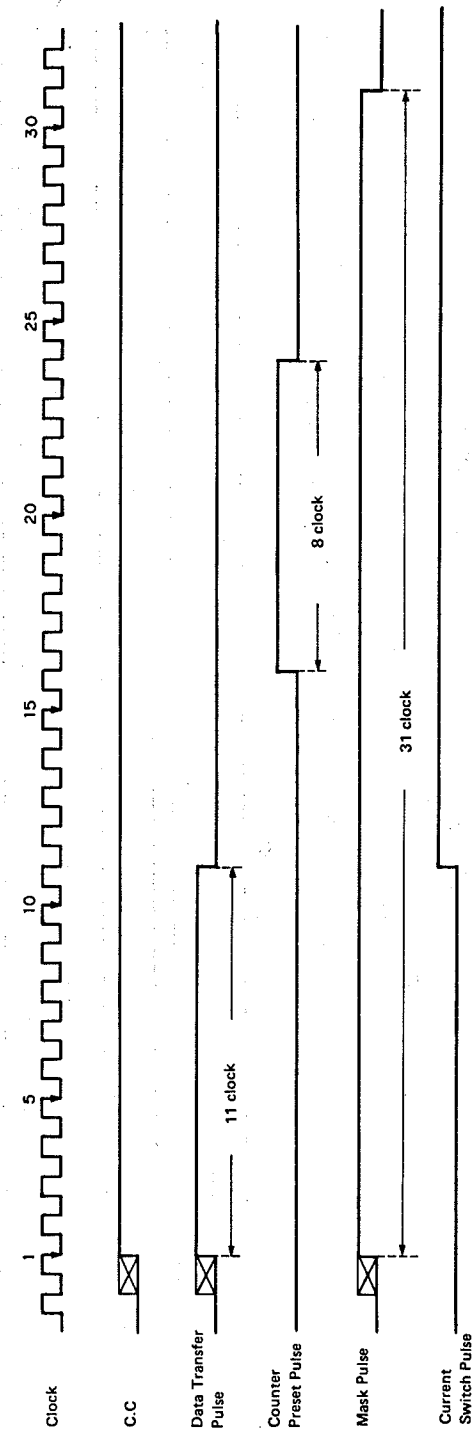


Fig. 2

Stereo Mode

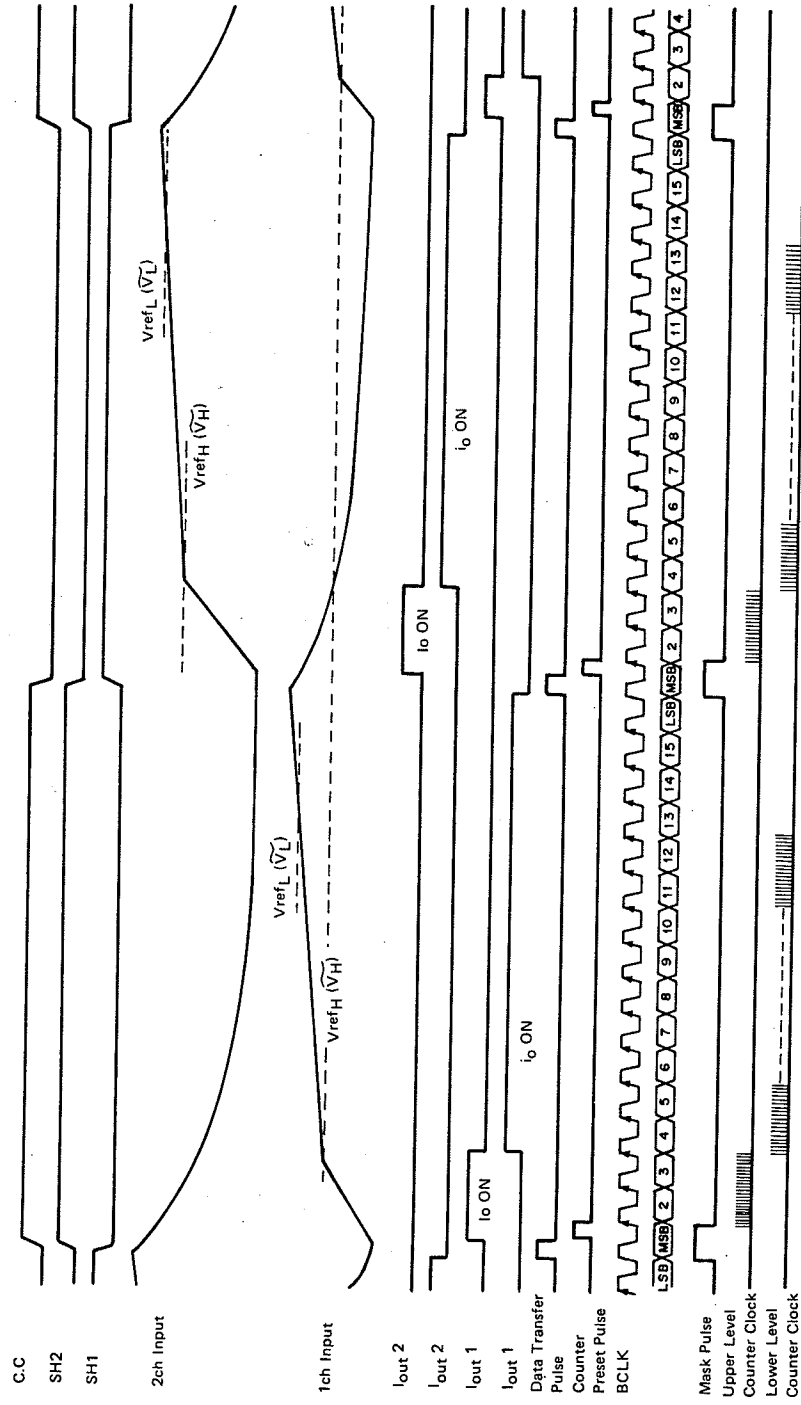


Fig. 3

Monaural Mode

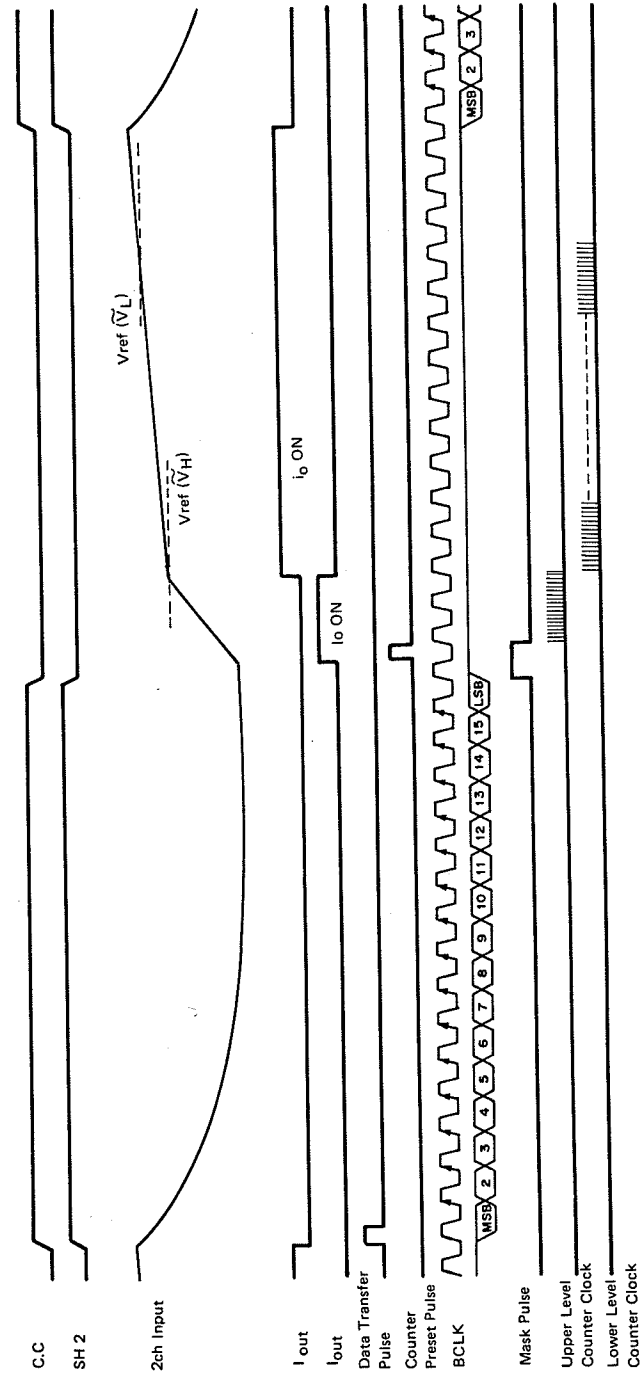


Fig. 4

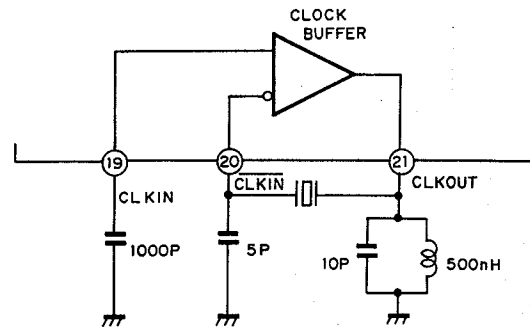
Interface Circuit, Divider Circuit, Sample Hold Circuit

(1) Integral current output

Recommended value; $I_{set} = 410 \mu A$
 $I_o = 4 I_{set} = 1.64 \text{ mA}$
 $I_o = \frac{1}{32} I_{set} = 12.8 \mu A$
 $I_{set} = 750 \mu A$
 at $C = 1000 \text{ pF}$ $f_{MCLK} = 84.6 \text{ MHz}$ full scale 10V

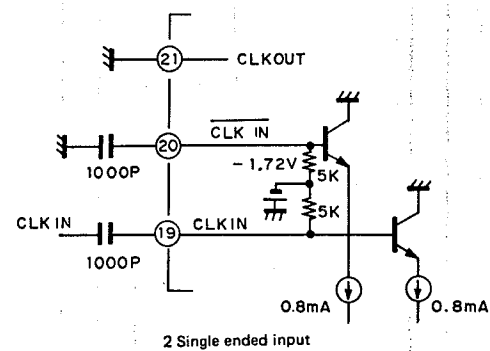
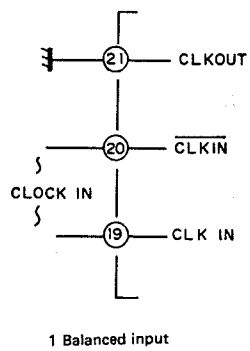
(2) Clock Buffer

(a) Internal clock (Excited circuit with crystal)



(X'tal 84.6 MHz)

(b) External clock



Select guide of master clock frequency

- Maximum operation clock frequency 100 MHz
- The minimum number of clock for a conversion is calculated as follows.

$$(2^9 - 2) + 2 \times (2^7 - 1) + (2^5 - 1) = 795 \text{ clocks}$$

Upper level Counter Timing circuit
 Lower level counter

In case of conversion frequency of 44.06 kHz,

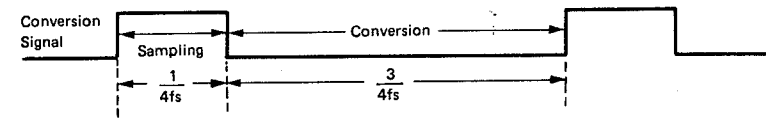
$$2f_s \times 795 = 70.1 \text{ MHz} \quad f_s: \text{Sampling frequency}$$

$f_{MCLK} \cong 71 \text{ MHz}$ (Conversion time is assigned 1/2 of period.)

- Conversion time is assigned 3/4 of a period in monaural mode.

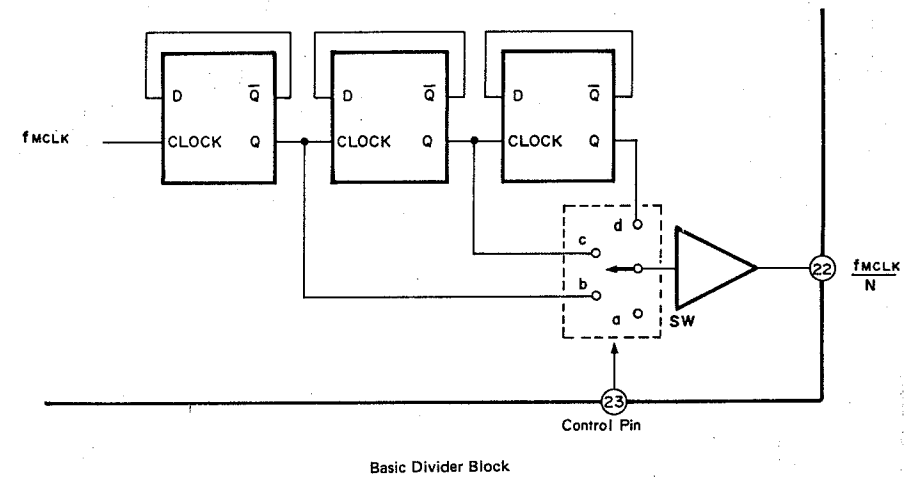
$$f_{MCLK} \cong 48 \text{ MHz}$$

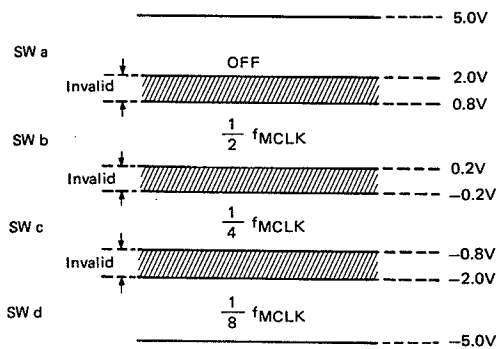
Note; See as follows



(3) f_{MCLK}/N Output

The output of f_{MCLK}/N is prepared for synchronous operation with digital circuit. Divided Value "N" is determined by external control, and N is 2, 4, 8 or ∞ .



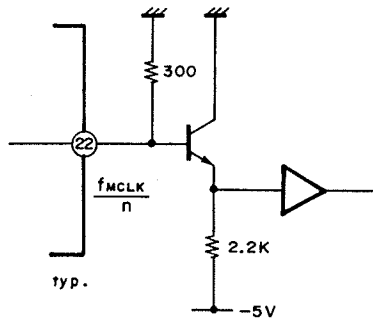


N	V _{CTL} Range
∞	$5.0V \geq V_{CTL} \geq 2.0V$
2	$0.8V \geq V_{CTL} \geq 0.2V$
4	$-0.2V \geq V_{CTL} \geq -0.8V$
8	$-2.0V \geq V_{CTL} \geq -5.0V$

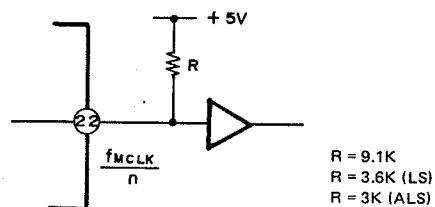
Threshold value of Control Pin

(4) Recommended Interface Circuit

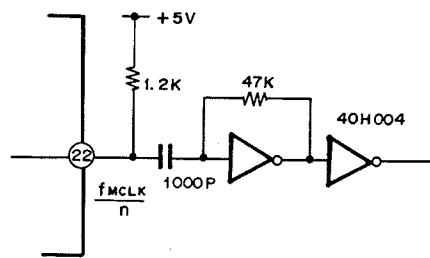
(a) ECL 10k (N=2)



(b) TTLs (N=4 or 8)



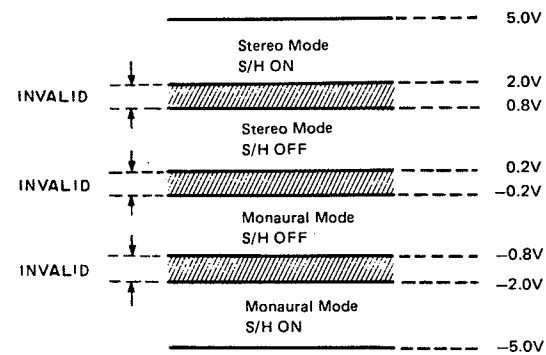
(c) High Speed CMOS (N=8)



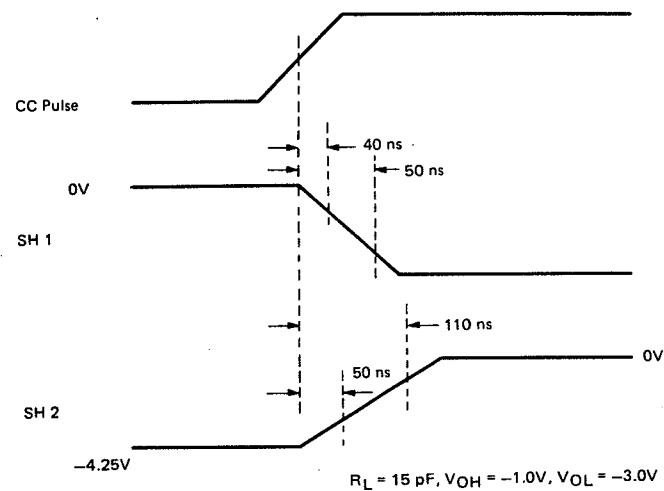
(5) Stereo mode, Monaural mode

Stereo or Monaural modes can be selected by mode pin. And "ON" or "OFF" state of Sample Hold Pulse is selected similarly.

This is illustrated in the following way.

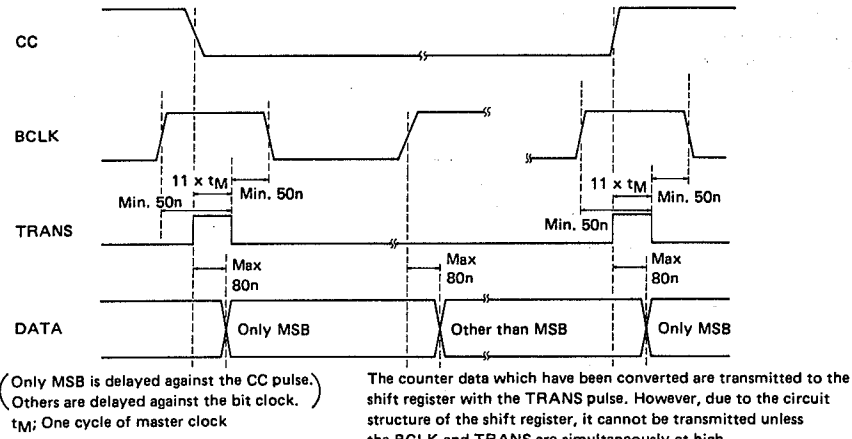


S/H Pulse



Propagation Delay Times from CC input to SH1, SH2 output

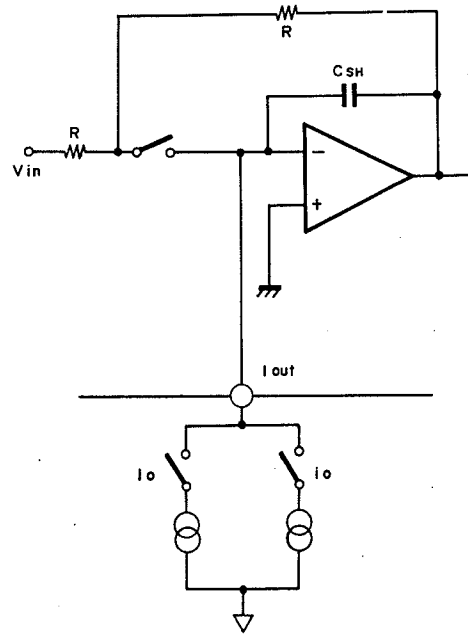
(6) Data Out



Propagation Delay Time from CC or BCLK Data Out

(7) Relationship of V_{in max}, C_{SH}, I_{set}, I_o and i_o

- (1) V_{in} is defined as the input voltage of integrator.
- (2) I_o, i_o are defined as the coarse and fine integral current respectively.
- (3) In case of a full scale input voltage.



$$V_{in \max} = \frac{I_o \tau_o}{C_{SH}} (2^9 - 1) + \frac{I_o \tau_o}{C_{SH}} (2^7 - 1)$$

$$\text{Using } I_o = 4 I_{set}, i_o = \frac{1}{32} I_{set}$$

$$V_{in \max} = \frac{1}{32} \cdot \frac{I_{set} \tau_o}{C_{SH}} (2^{16} - 1)$$

$$\text{Assuming } V_{in \max} = 10 \text{ Vp-p}, \tau_o = \frac{1}{f} = \frac{1}{84.6 \text{ MHz}}$$

$$C_{SH} = 1500 \text{ PF}$$

$$\therefore I_{set} = 620 \mu\text{A}$$

$$\therefore 1 \text{ LSB} = \frac{I_o \tau_o}{C_{SH}} = 152 \mu\text{V}$$

Note) In case of non-inverting operation, V_{in Max.} is limited to 5 Vp-p.

(8) The maximum frequency of BCLK.

The maximum frequency of BCLK is derived as follows:

$$f_{BCLK} = \frac{1}{2t_{BH}}$$

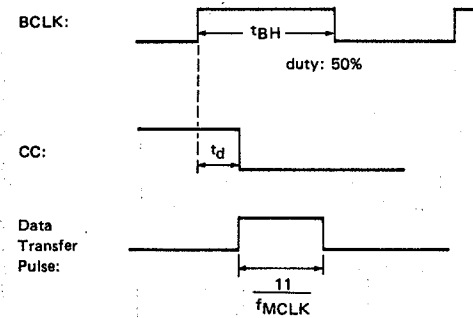
$$t_{BH} \cong t_d + \frac{11}{f_{MCLK}} + 50 \text{ ns}$$

$$0 \text{ ns} \cong t_d \cong 100 \text{ ns}$$

Therefore,

f_{BCLK} ≅ 1.7 MHz on condition that the duty of BCLK is 50%.

f_{BCLK} ≅ 1.7 × $\frac{50}{X}$ MHz on condition that the duty is X%.



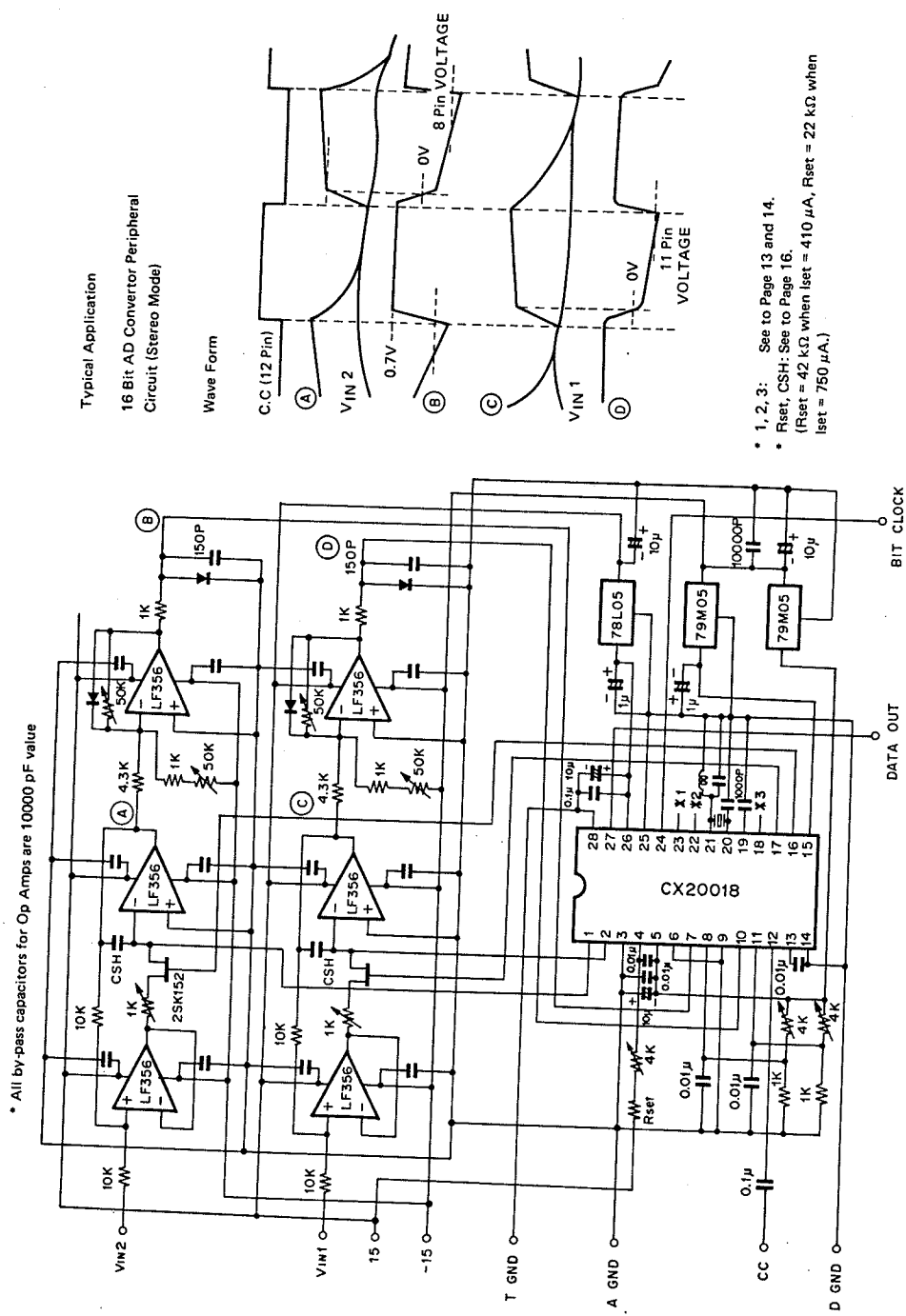
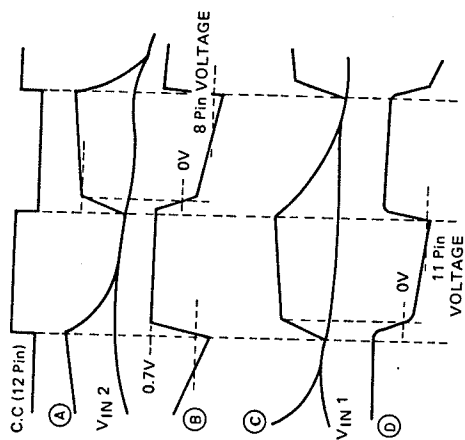


Fig. 5 16 bit A/D Converter Peripheral Circuit (Stereo Mode)

- 1, 2, 3: See to Page 13 and 14.
- Rset, CSH: See to Page 16.
(Rset = 42 kΩ when Iset = 410 µA, Rset = 22 kΩ when Iset = 750 µA.)

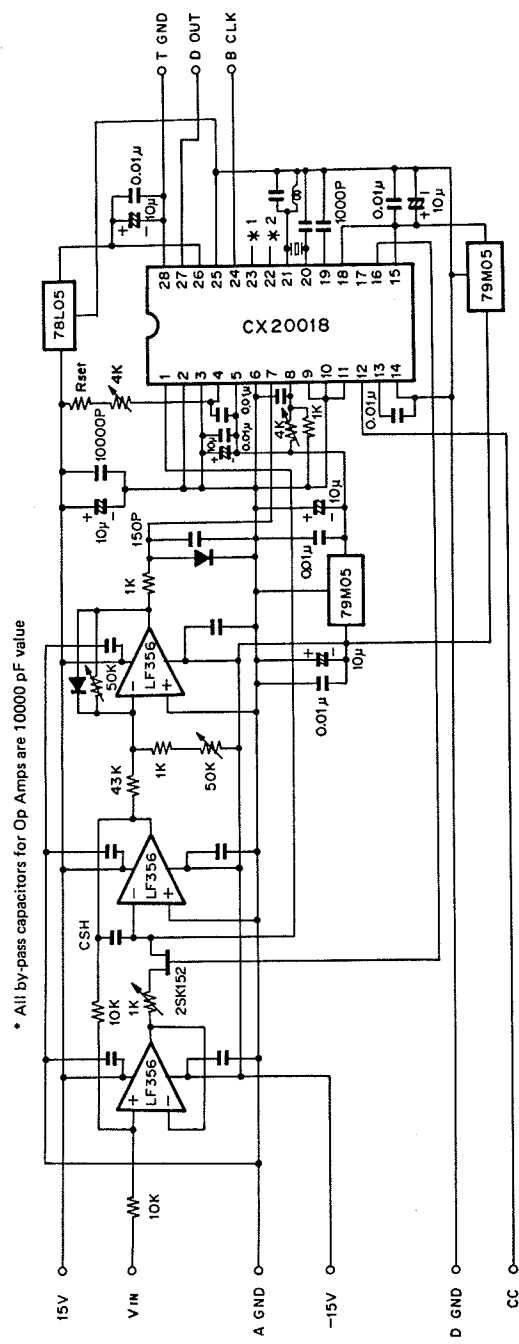
Typical Application
16 Bit AD Converter Peripheral
Circuit (Stereo Mode)

Wave Form



Typical Application - Monaural Mode

16 Bit AD Converter Peripheral Circuit (Monaural Mode)



- 1, 2: See to Page 13 and 14.
- Rset, CSH: See to Page 16 (Rset = 42 kΩ when Iset = 410 µA, Rset = 22 kΩ when Iset = 750 µA).

Fig. 6 16 bit A/D Converter Peripheral Circuit (Monaural Mode)

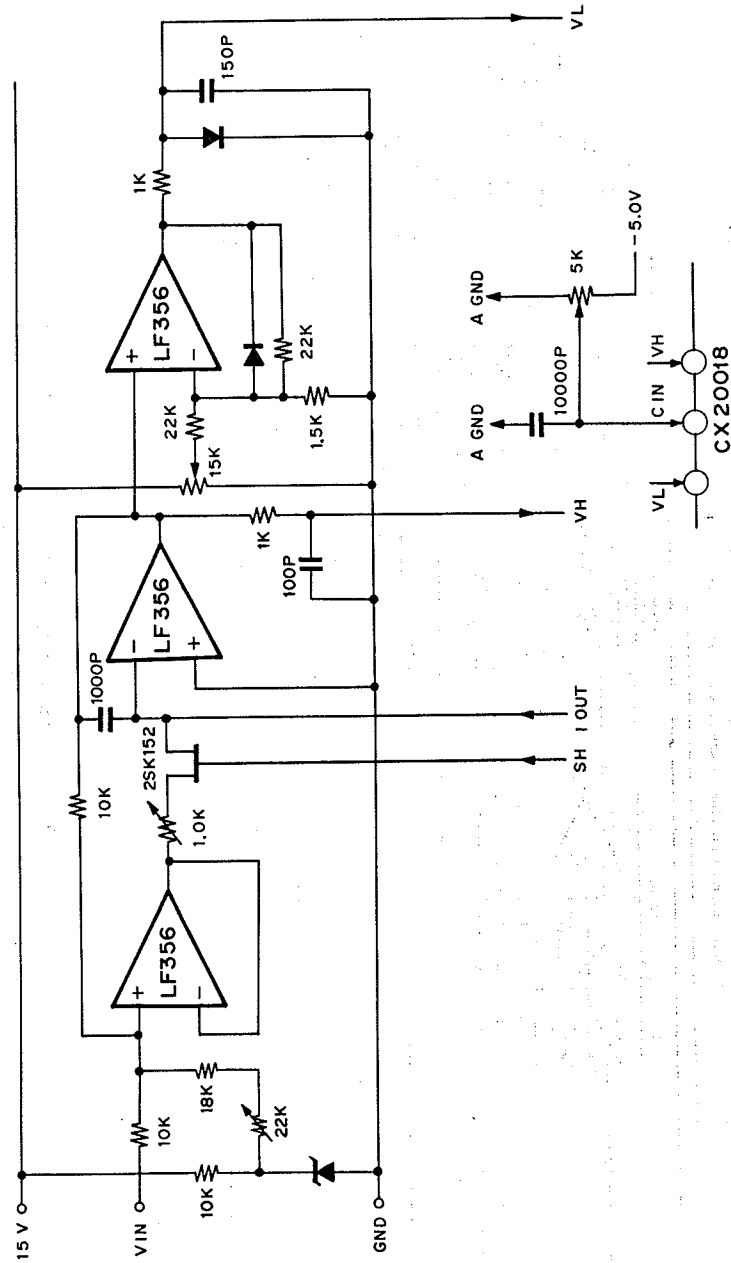


Fig. 7 Application Circuit (Non-inverting Circuit)

